On abstraction and compositionality for weak-memory linearisability

Brijesh Dongol Radha Jagadeesan James Riely
Alasdair Armstrong

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    — captures a large number of memory models (TSO, Power, ARM)
  - Concurrent objects (this paper)
  - Transactional memory (Dongol, Jagadeesan and Riely, POPL 2018)

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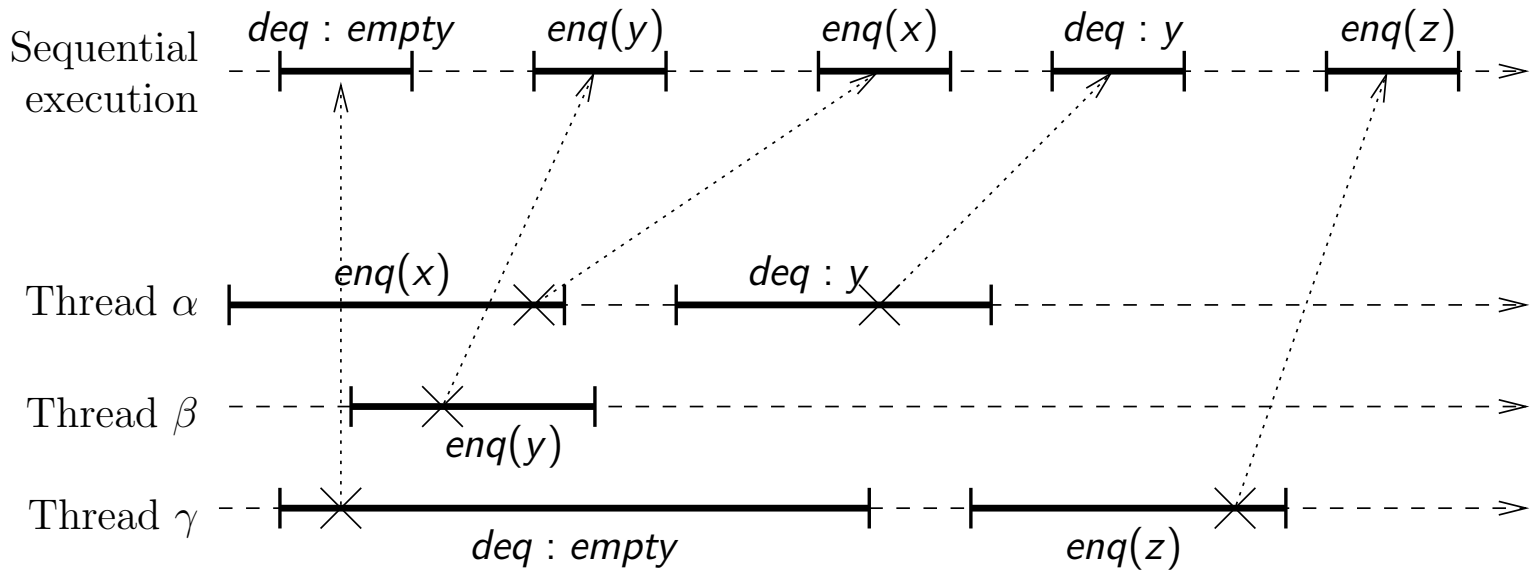

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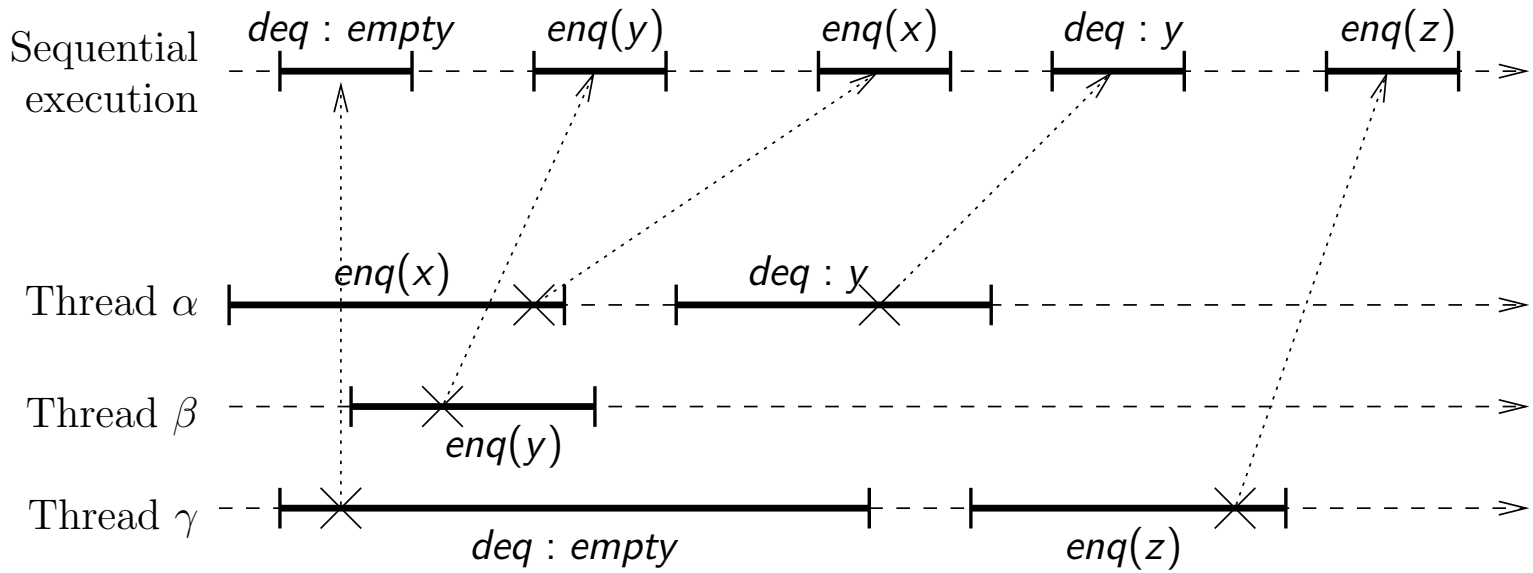

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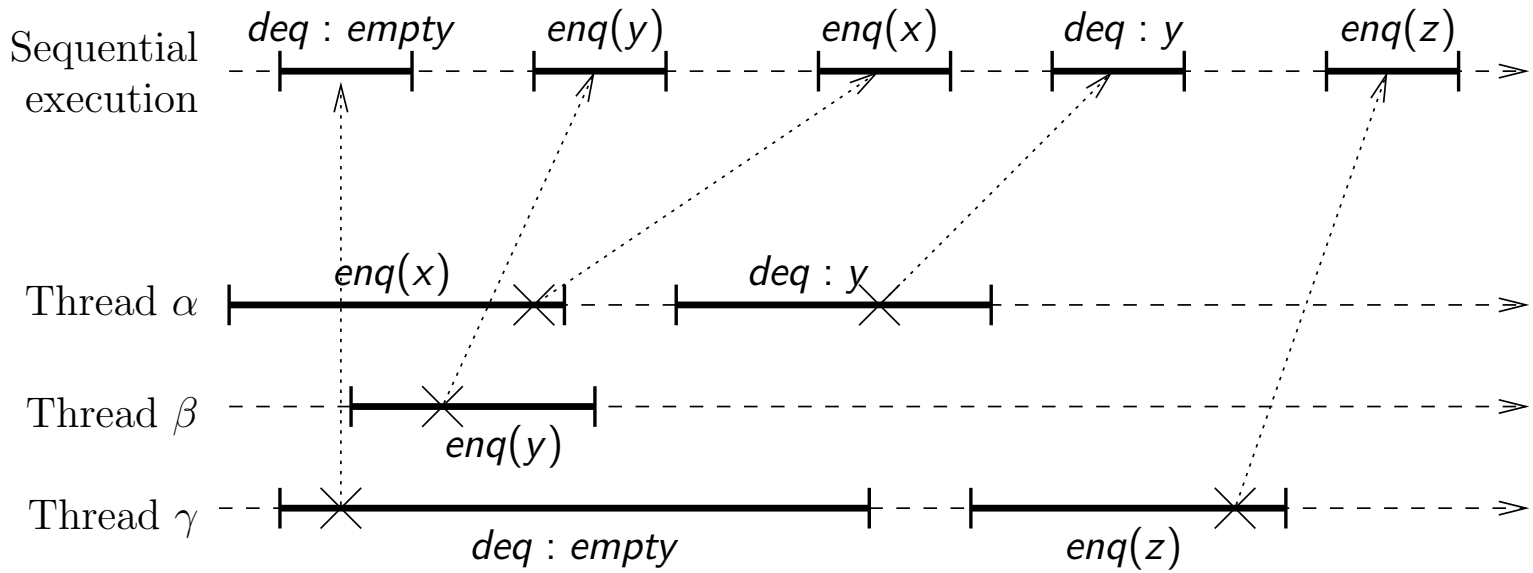

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- What about weak memory?

AMT's axiomatic models

Executions defined by:

- Set of (read/write) *events* $\mathbb{E}$ and *orders* over $\mathbb{E}$, e.g.,
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Execution is correct if it satisfies four axioms:

$$\mathsf{acyclic}(\mathsf{hb}) \qquad \text{(No-Thin-Air)}$$

$$\mathsf{acyclic}(\mathsf{po\text{-}loc} \cup \mathsf{co} \cup \mathsf{rf} \cup \mathsf{fr}) \qquad \text{(SC-Per-Location)}$$

$$\mathsf{irreflexive}(\mathsf{fre}; \mathsf{prop}; \mathsf{hb}^*) \qquad \text{(Observation)}$$

$$\mathsf{acyclic}(\mathsf{co} \cup \mathsf{prop}) \qquad \text{(Propagation)}$$

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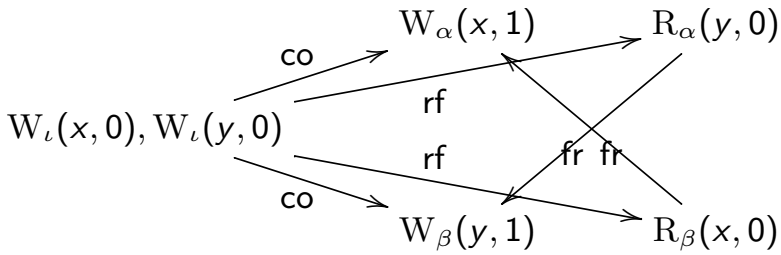

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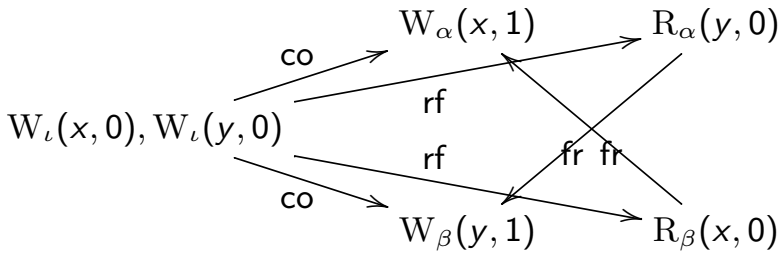

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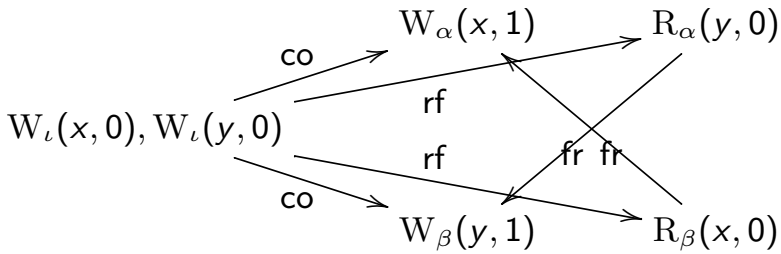

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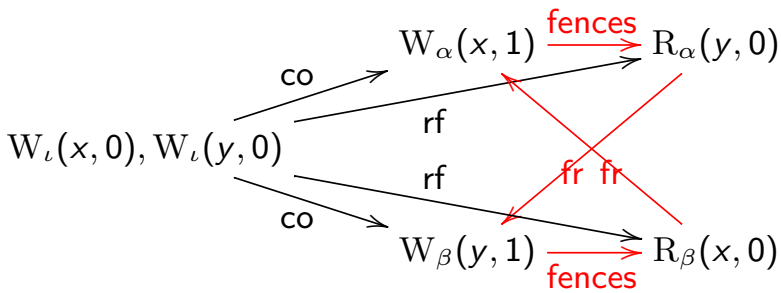

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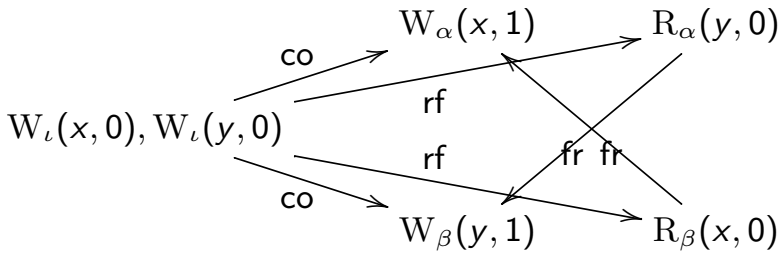

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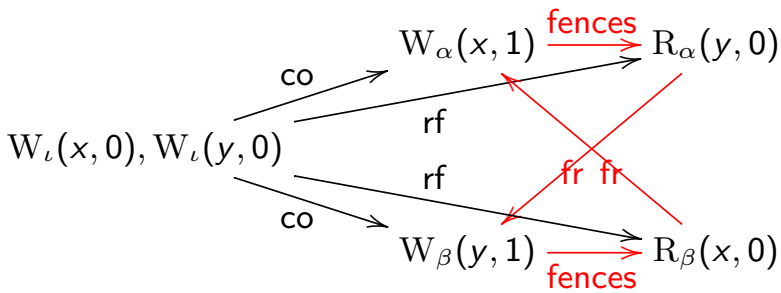

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Let's apply this framework to a setting with concurrent objects

Abstract objects and weak memory

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Init:  x, y = 0, 0
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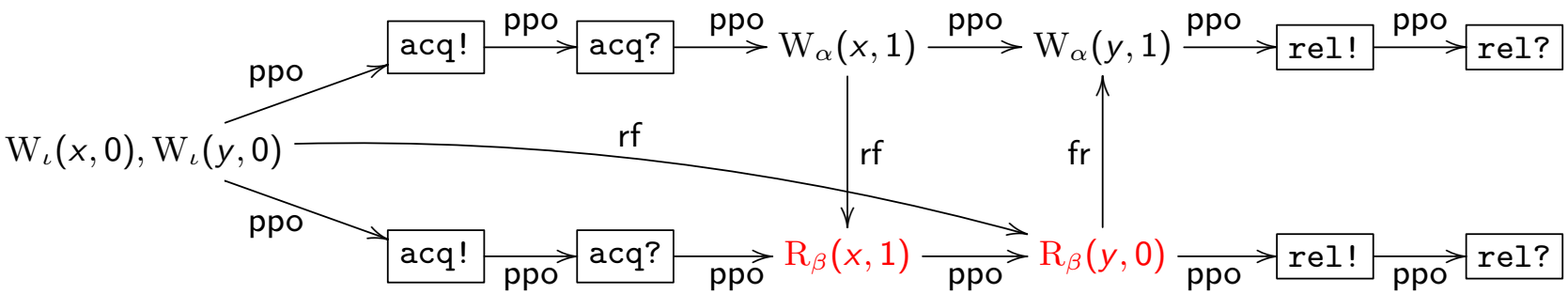

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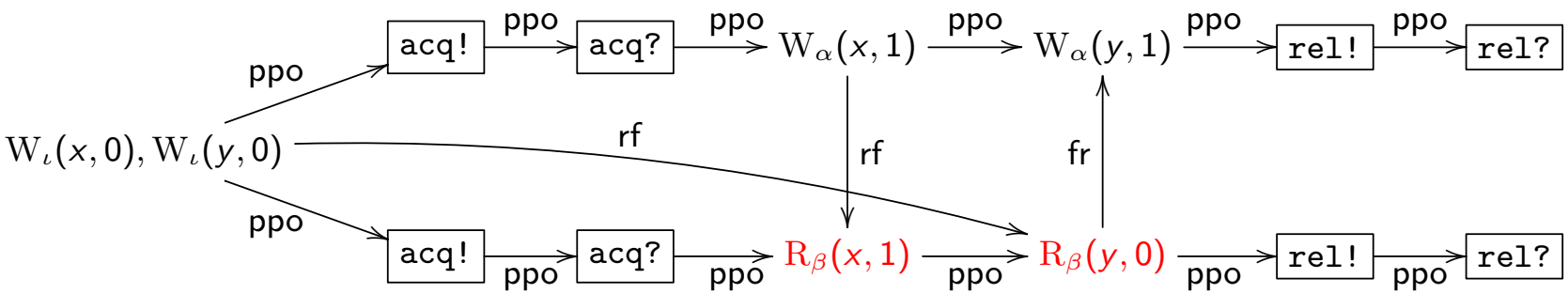

Allowed execution

- Two problems:
  1. Typical SC lock specification is not strong enough
     - Only describes allowable order of operations
     - Doesn't describe memory effects
  2. Weak memory axioms ignore interaction with lock object

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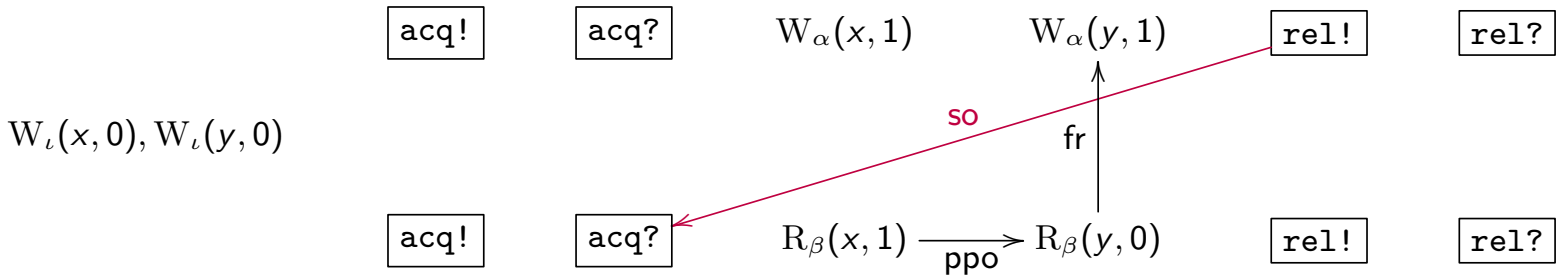

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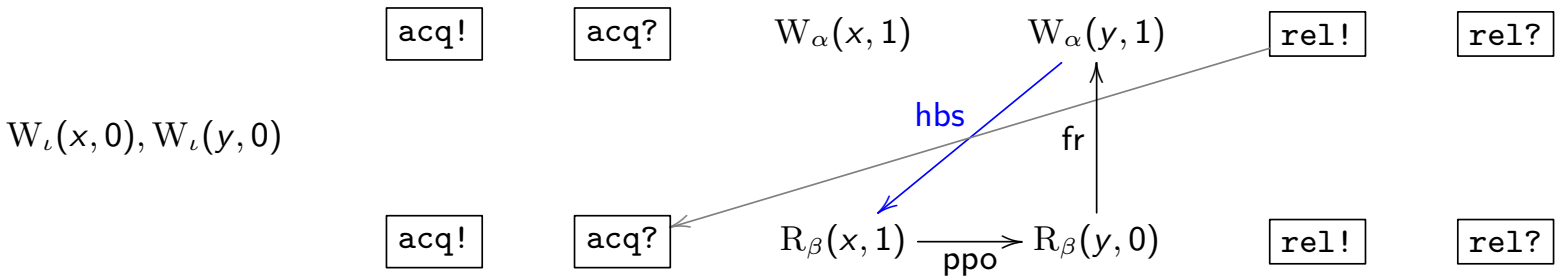

Violates OBSERVATION axiom

1. Strengthen the lock specification to include specification order (so) from release to acquire
2. Strengthen the weak memory axioms to induce additional happens before (hbs)

Strengthening specifications

- Under SC, a specification defined by legal history

  Example. Legal stack history (ensures LIFO order)

  $$a : push!(5) \cdot a : push? \cdot b : push!(6) \cdot b : push? \cdot c : pop! \cdot c : pop?(6)$$

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- Specification order is used to build additional happens-before

  $$\mathsf{hbs} \quad = \quad \mathsf{po}; \mathsf{so}; \mathsf{po}$$

Abstract executions via example (publication)

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Init:  x = 0
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Possible (bad) abstract trace of this client/object program:

$$\mathrm{W}_\alpha(x,5) \quad \mathit{push}!_\alpha(5) \quad \mathit{push}?_\alpha$$

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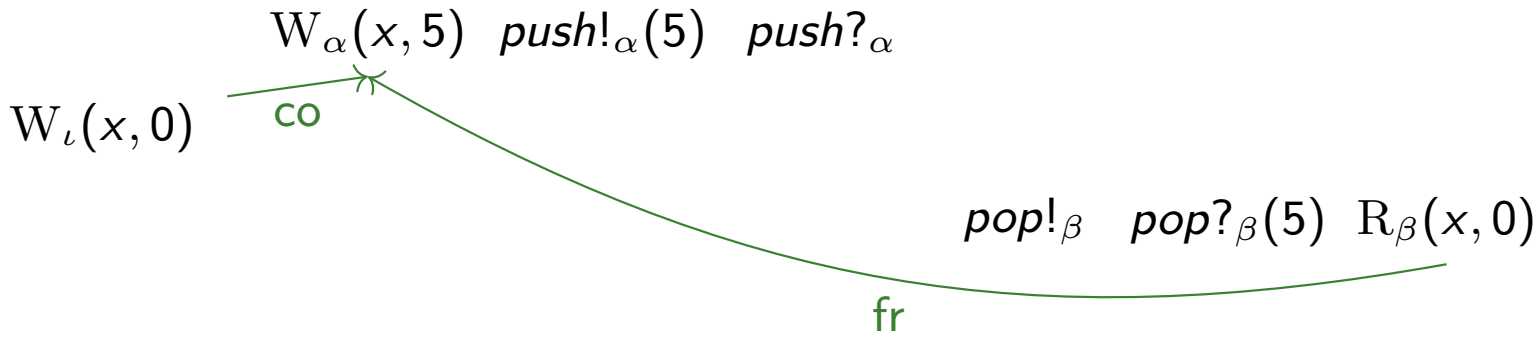

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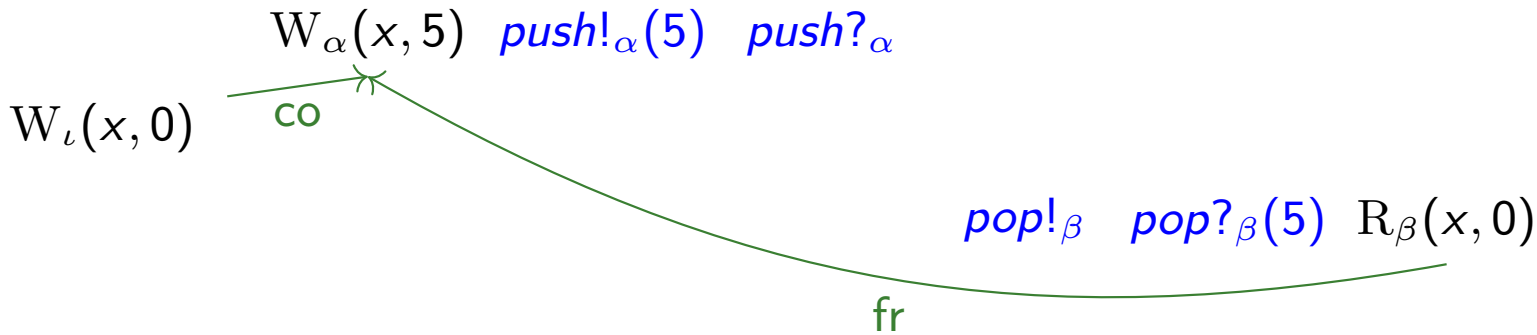

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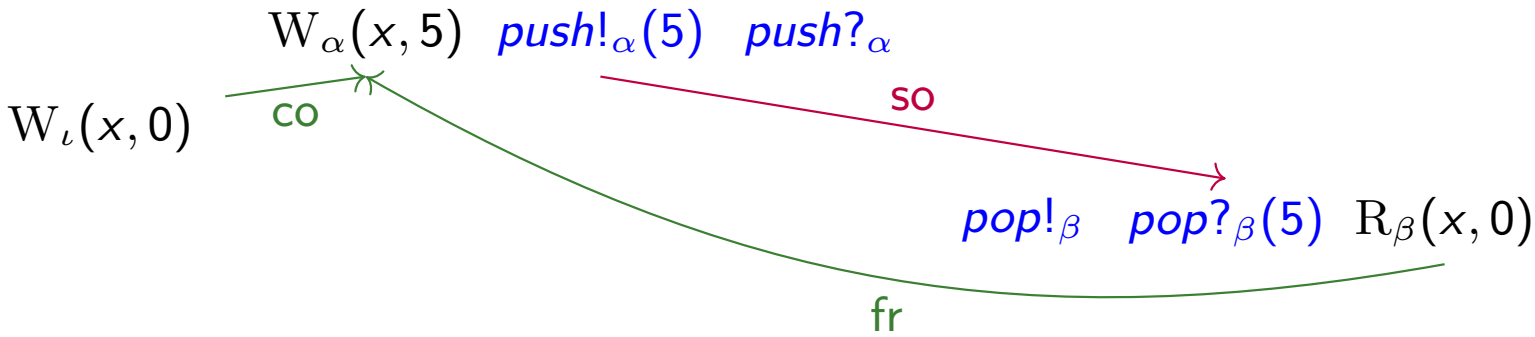

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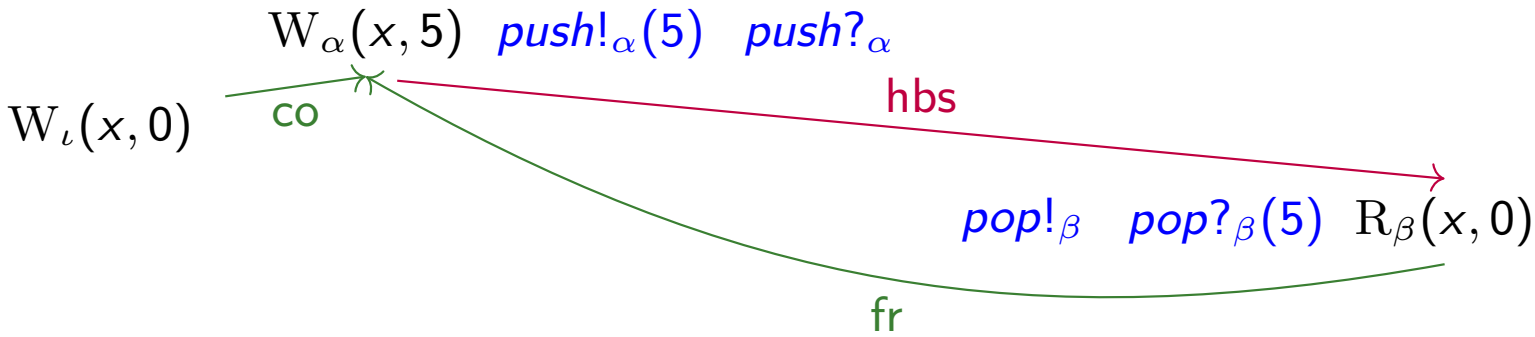

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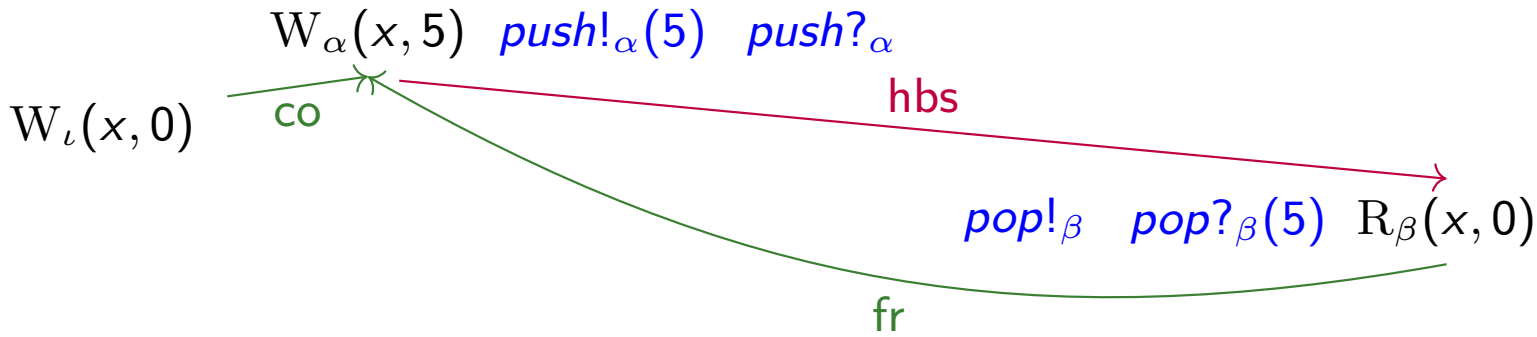

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5. Execution is invalid (as desired) according to AMT axioms using

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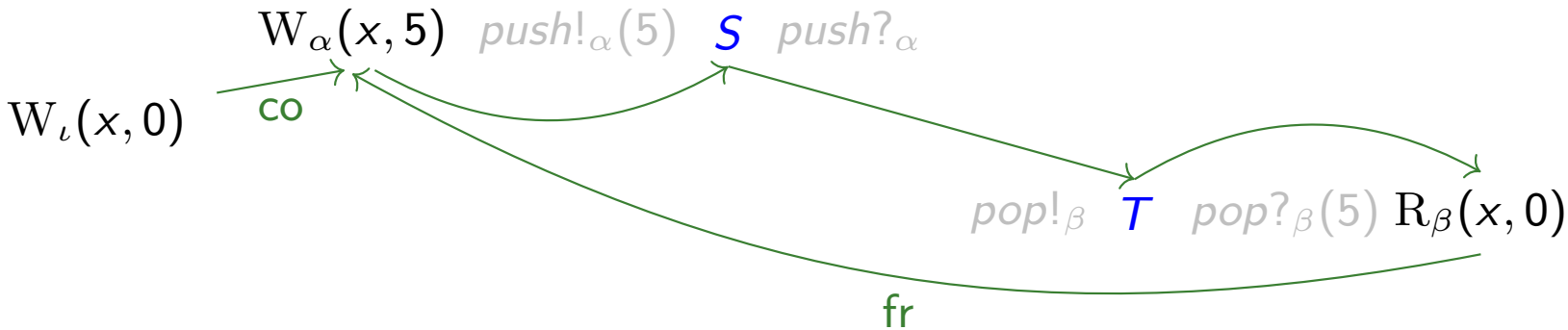

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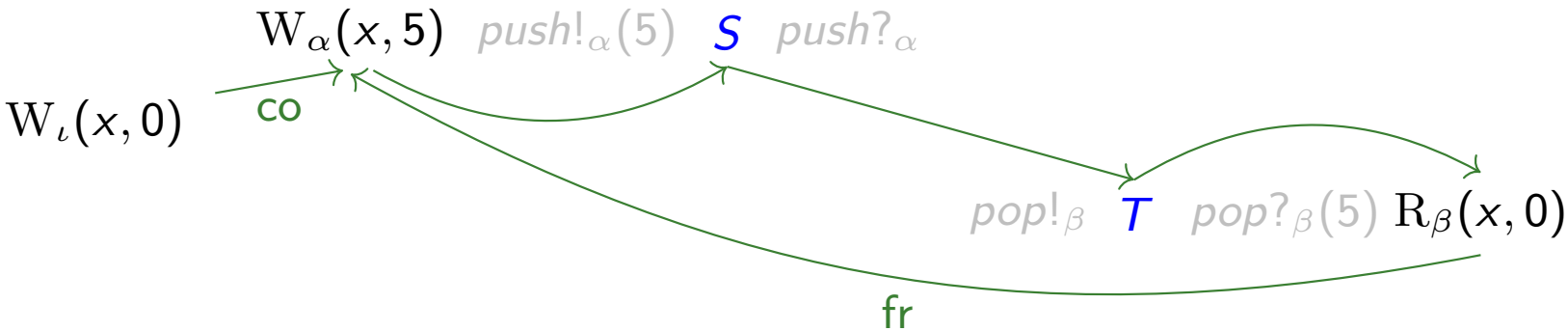

- If the stack is correct, then there must be memory actions in S, T that invalidates the execution
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- But we want to think about clients and object implementations separately
- Use the abstract specification as the glue

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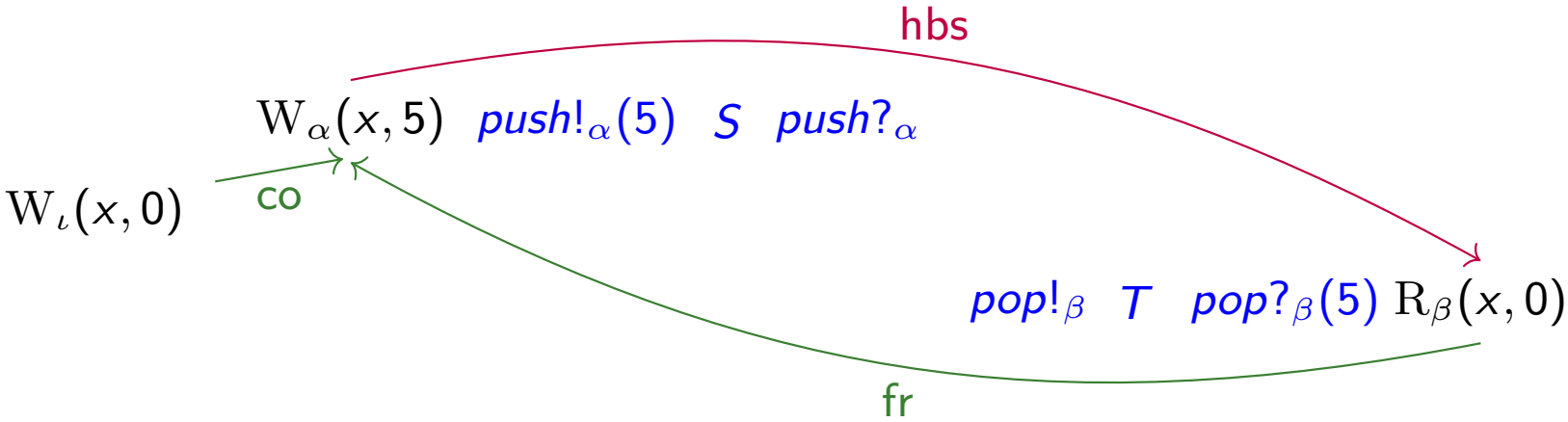

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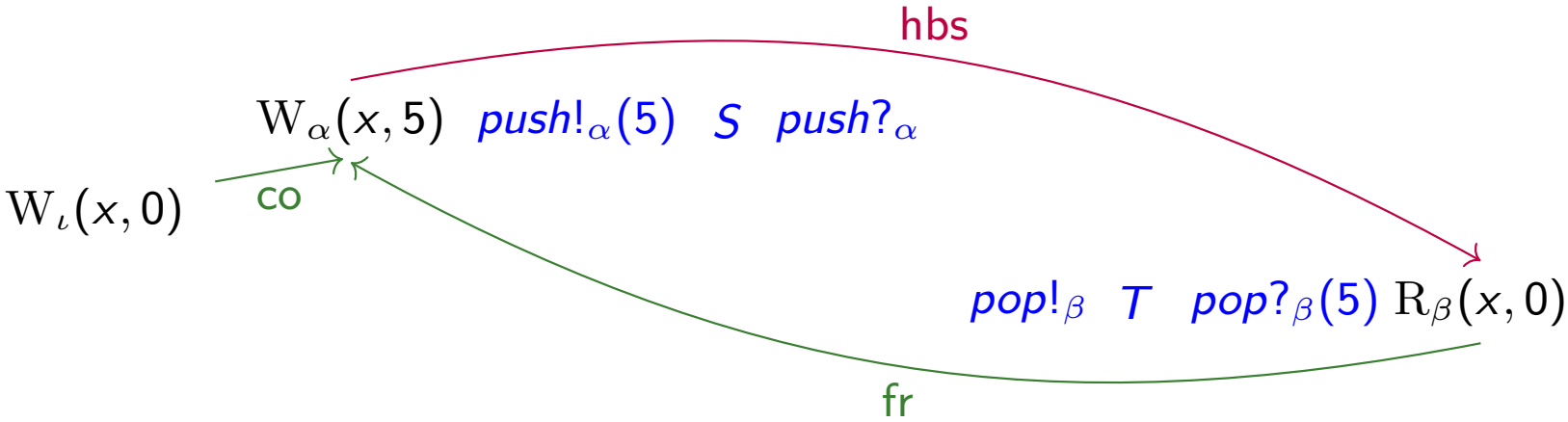

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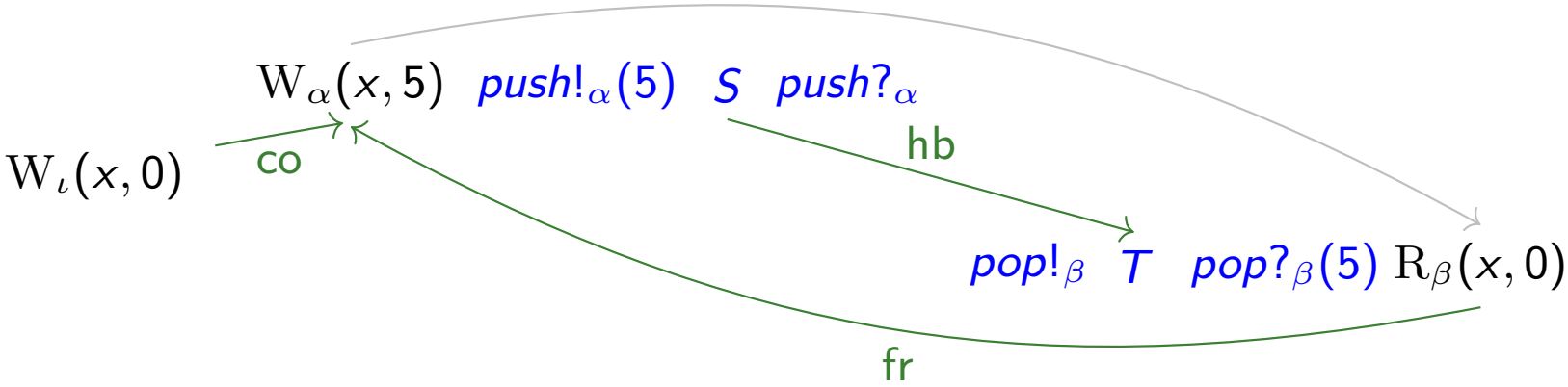

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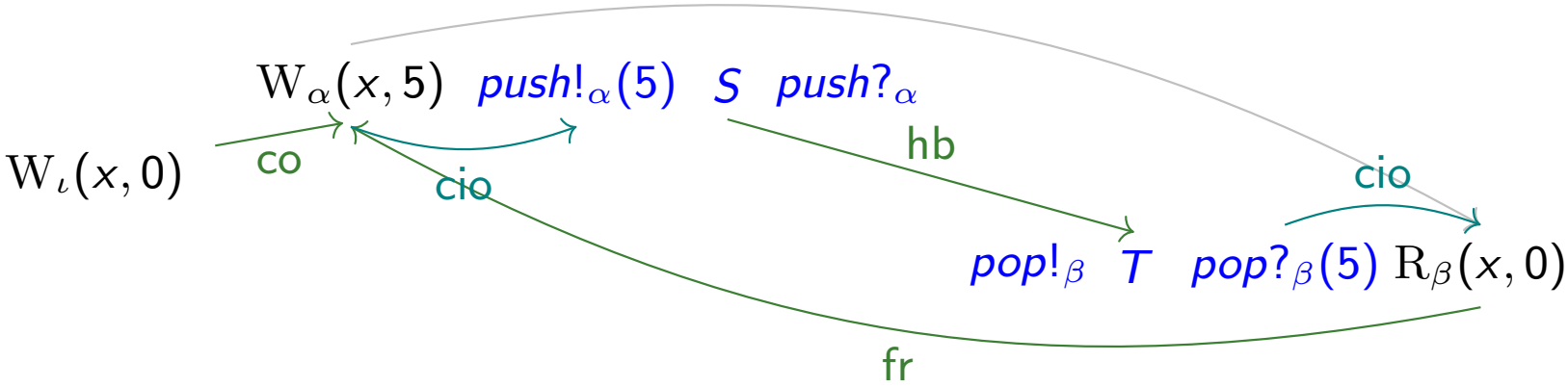

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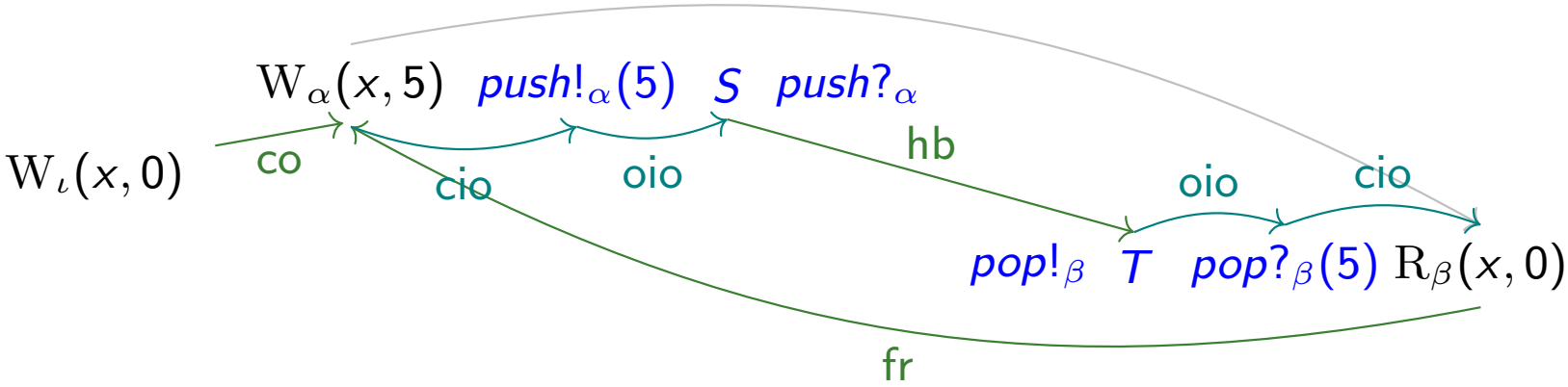
  2. client-interface order (cio):
     - client events to invocations and
     - responses to client events

Concrete implementations



- Recall: We require hbs to create a cycle using a from read anti-depedency
- Problem: How do we ensure hbs exists
  - without knowledge of client (reasoning about the object only),
  - generically for any memory model?
- Three sets of edges to consider
  1. hb order from S to T (given by the memory model)
  2. client-interface order (cio):
     - client events to invocations and
     - responses to client events
  3. object-interface order (oio):
     - invocations to object events, and
     - object events to responses

Preventing artificial order

- We cannot, by default, include both $\xrightarrow{\text{cio}}$ and $\xrightarrow{\text{oio}}$

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Program 1 in TSO

```
Thread α:  x:=1; r:=y
```

$\mathrm{W}_\alpha(x,1) \qquad \mathrm{R}_\alpha(y,0)$

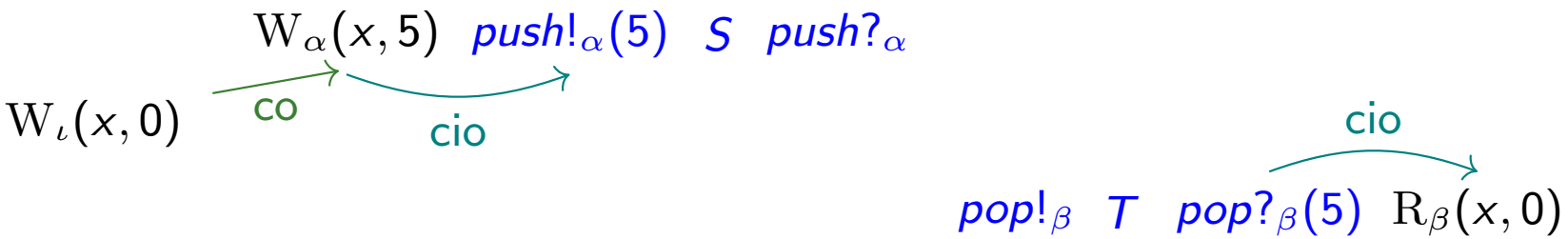
Program 2 in TSO

```
Thread α:  x:=1; empty(); r:=y
```

$\mathrm{W}_\alpha(x,1) \xrightarrow{\text{cio}} E! \xrightarrow{\text{oio}} E? \xrightarrow{\text{cio}} \mathrm{R}_\alpha(y,0)$

- **Solution.**
  - By default assume: ClientEvent $\xrightarrow{\text{cio}}$ Invocation
  - Conditionally have: Invocation $\xrightarrow{\text{oio}}$ ObjectEvent

Object interface orders (oio) in example



- A correct stack implementation must guarantee:
  1. $S \xrightarrow{\text{hb}} T$
  2. $push!_\alpha(5) \xrightarrow{\text{oio}} S$
  3. $T \xrightarrow{\text{oio}} pop?_\beta(5)$

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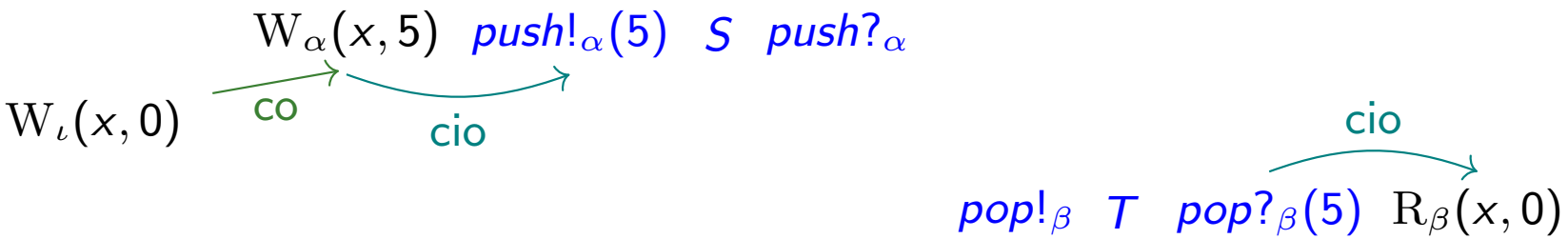

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  2. $push!_\alpha(5) \xrightarrow{\text{oio}} S$
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- Reasoning above entirely contained within the object
- All orders stem from the memory model

Programmer expectation

- Want a condition Z such that for any
  - abstract object AS and
  - concrete object CS

$$Z(AS, CS) \quad \Rightarrow \quad \forall C \in \mathit{Client}.\ C[AS] \sqsubseteq C[CS] \qquad \text{(Abstraction)}$$

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- We develop two instantiations of Z:
  - real-time hb-linearisability
  - causal hb-linearisability

Real-time hb-linearisability

Definition

Client-implementation trace t *real-time* hb-*linearisable* with respect to (h, so) if

$$\forall \alpha \in \mathit{Threads}.\ t|(\mathbb{I} \cup \mathbb{R})|\alpha = h|\alpha \qquad \text{(Permutation)}$$

$$\forall i \in \mathbb{I}, r \in \mathbb{R}.\ r \xrightarrow{t} i \ \Rightarrow\ r \xrightarrow{h} i \qquad \text{(RTO-Preservation)}$$

$$\forall i \in \mathbb{I}, r \in \mathbb{R}.\ i \xrightarrow{\mathsf{so}} r \ \Rightarrow\ i \xrightarrow{\mathsf{hb}^+} r \qquad \text{(HB-Satisfaction)}$$

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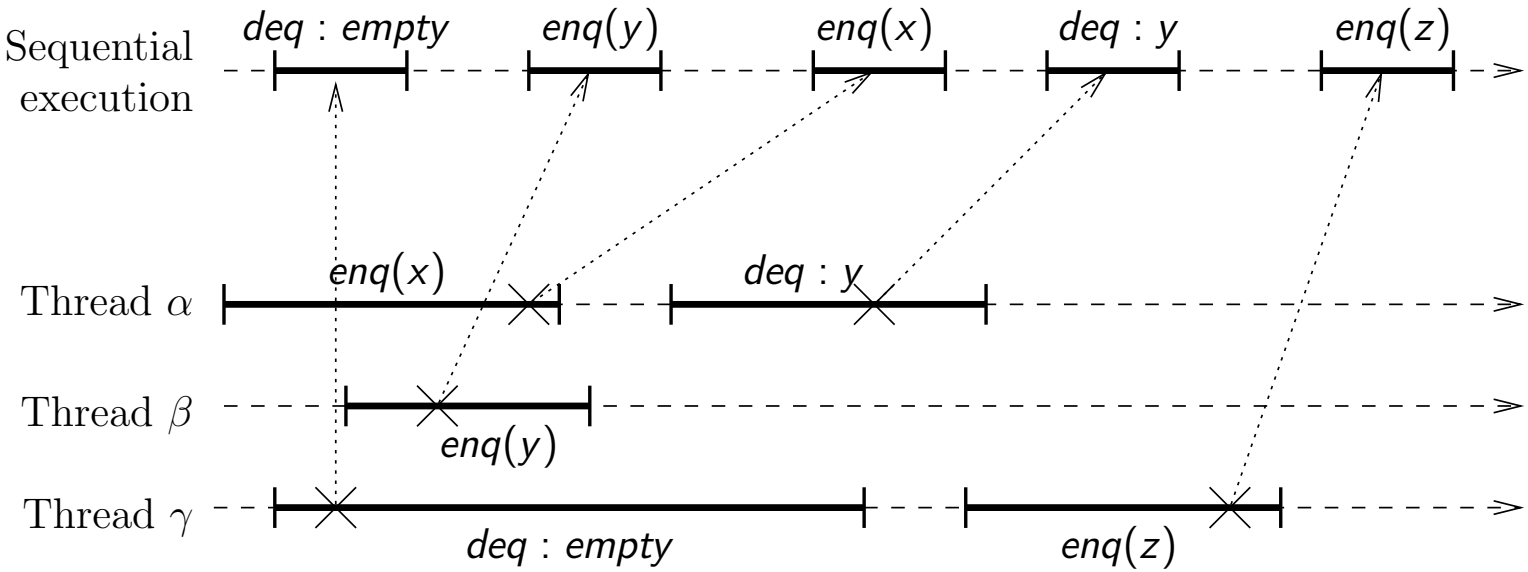

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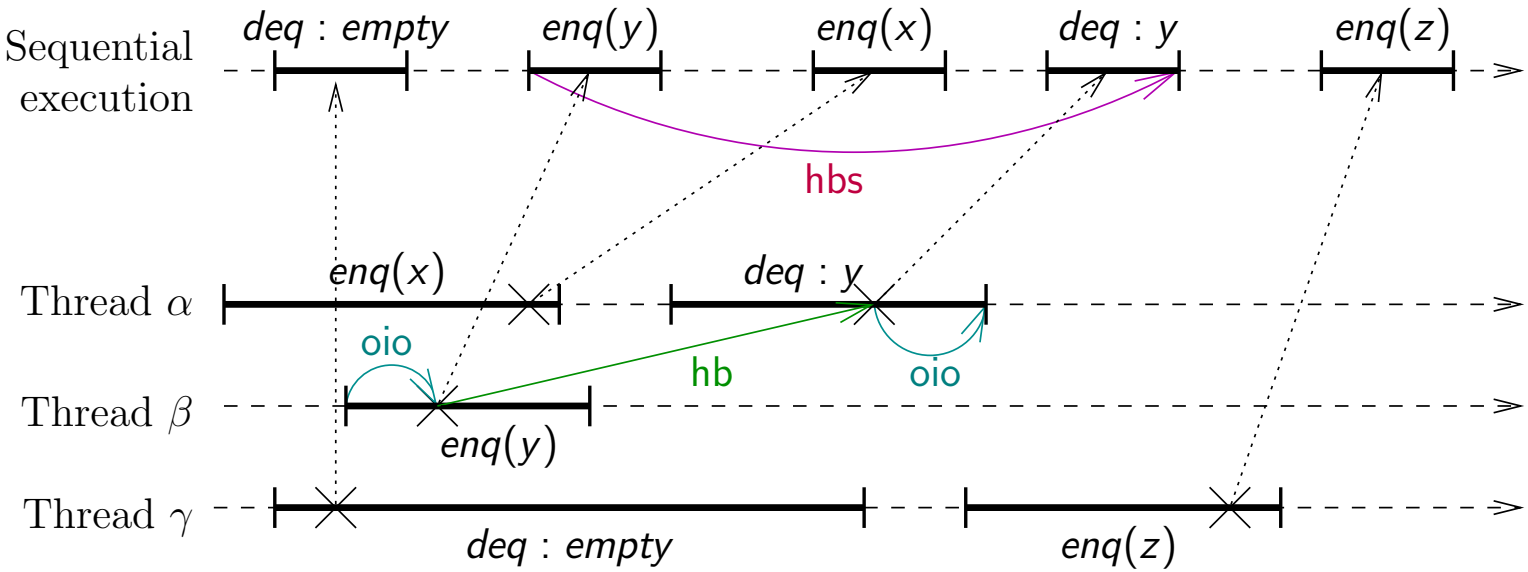

Causal hb-linearisability

- In the weak memory setting, there is an opportunity to relax the real-time order constraint
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Definition

Implementation trace t is *causal* hb-*linearisable* with respect to (h, so) iff

$$\forall \alpha \in \mathit{Threads}.\ t|(\mathbb{I} \cup \mathbb{R})|\alpha = h|\alpha \qquad \text{(Permutation)}$$

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Abstraction and compositionality

- Both real-time and causal hb-linearisability guarantee abstraction
- Real-time hb-linearisability ensures compositionality
- Compositionality for causal hb-linearisability requires either
  - an unobtrusive client, or
  - a commutative specification

Our paper

Contributions:

1. Extension of AMT model to cope with client-object programs
2. Enable objects to be developed independently of client:
   - Real-time hb-linearisability
   - Causal hb-linearisability
3. Abstraction and compositionality theorems for both forms of linearisability

Benefit: Applicable to many different memory models: TSO, Power, ARMv7 ...

Questions?